6. WHAT IS CLAIMED IS:

1. A recording format for information data in a magnetic recording/reproduction apparatus, wherein:

a recording code sequence format recorded on a recording medium comprises:

a preamble including additional information for the control of recorded position information, amplitude gain control and data timing recovery;

an information code composed of plural code blocks including second redundant code bits (second parity code bits); and

a redundant code composed first redundant code bits for data error correction (first parity code bits); and

the length (number of code symbols) of each code block including redundant code bits in the second redundant code is equal to or shorter than a number of code symbol units correctable by the first redundant code bits.

2. A recording format for information data according to Claim 1, wherein:

the second redundant code bits (the parity code bits) are collectively recorded in predetermined positions in each code block.

3. An information recording/reproducing encoding circuit provided with an error-correction encoding circuit that applies coding for correcting code errors caused when an information code sequence is

reproduced from an information recording medium to the information code sequence recorded onto the information recording medium, comprising:

a first encoding circuit that applies first error-correction coding to a unit of an input information code sequence (an information data sector) once recorded on the information recording medium in units of predetermined code (code symbol) and executes the first error-correction coding for correcting the error code symbols equal or smaller than a predetermined number of code symbols, which are caused in the corresponding reproduced sector;

a circuit that adds a redundant code sequence by the first error-correction coding to the information data sector hereby output, divides the contents of code sequence of the information data sector code sequence output from the first encoding circuit (that executes the first error-correction coding )into continuous plural code sequence blocks having predetermined length and holds them;

a second encoding circuit that executes second error-correction coding for each code sequence block, referring to the contents of each code sequence block held in the said circuit; and

an error-correction encoding circuit that outputs a series of code sequence block as a code sequence recorded on the information recording medium after redundant code bits output from the second encoding

circuit are inserted into the corresponding code sequence block, wherein the length of the code sequence block in units of code symbol is set to a length equal or shorter than the number of code symbols correctable by the first error-correction coding, wherein:

after a code sequence corresponding to information code sequence recorded on an information recording medium is converted by the error-correction encoding circuit, it is output from the encoding circuit.

4. An information recording/reproducing encoding circuit according to Claim 3, wherein:

the encoding circuit that executes the second error-correction coding comprises:

a code permutation circuit for processing a code sequence corresponding to the code sequence block in units of code length equal to the code sequence block;

memory circuits for holding the result of the code permutation in units of code length equal to the code sequence block;

encoding circuits that respectively executes predetermined second error-correction coding, referring to the contents of the memory circuits; and

circuit means that inserts redundant bits output by respective encoding circuits in a predetermined positions in the corresponding code sequence block held in the memory circuit beforehand.

5. An information recording/reproducing

encoding circuit according to Claim 4, comprising:

a soft-output decoder that receives a reproduced signal sequence supplied from the recording medium and outputs the soft-output information of each code bit to detect and correct code errors by the second error-correction coding, wherein:

each of plural error-correction decoding circuits that detect and correct a code error using each error-correction coding applied to each code sequence block receives soft-output information for each code bit output from the soft-output decoder, receives soft-output information output from another error-correction decoding circuit, repeats the error detection and correction at plural times for each code sequence block and outputs the result of the error detection and correction as the result of the reproduction of the information code sequence after the error detection and correction are repeated by a predetermined frequency.

6. An information recording/reproducing encoding circuit according to Claim 5, comprising:

a memory circuit that holds the contents of information data sector to which redundant codes are added by the first error-correction coding, which is a code sequence output from the encoding circuit that executes the first error-correction coding, an encoding permutation circuit that refers the contents of a code sequence in the information data sector, permutes them and outputs, an encoding circuit applies the second

error correction coding to the code sequence output from the encoding permutation circuit,a decoding circuit receives a reproduced signal sequence supplied from the recording medium in the detection and correction of a code error in the corresponding information data sector, receives soft-output information for each code bit acquired as a result of the code error detection and correction repeated by the second error correction coding at a predetermined frequency, outputs the information of soft-output decoding for each code bit again and repeats the second error-correction coding using this information of soft-output decoding.

7. An information recording/reproducing encoding circuit according to Claim 5, wherein:

the error code detection and correction by the first error-correction coding or the error code detection and correction of a code error by the second error-correction coding is repeated only in case in the error code detection and correction by the first error-correction coding, code errors are detected and all the code errors cannot be corrected.

8. An information recording/reproducing encoding circuit according to Claim 5, wherein:

an iteration frequency or the maximum iteration frequency of the error code detection and correction by the first error-correction coding or the error code detection and correction by the second error-correction

coding is set from the outside of the information recording/reproducing encoding circuit; and

a memory circuit for setting and holding it or a register and an interface circuit for setting it in the memory circuit is/are provided.

9. An information recording/reproducing encoding circuit according to Claim 5, wherein:

an iteration frequency or the maximum iteration frequency of the error code detection and correction by the first error-correction coding and the error code detection and correction by the second error-correction coding are set from the outside of the information recording/reproducing encoding circuit; and

a memory circuit for setting and holding it or a register and an interface circuit for setting it in the memory circuit is/are provided.

10. An information recording/reproducing encoding circuit according to Claim 5, wherein:

when signal amplitude loss (dropout) with a predetermined code length is added to a reproduced signal sequence supplied from the recording medium or when a set iteration frequency is increased, time interval since the reproduced signal sequence is input to the encoding circuit until the decoding result of an information code sequence for the reproduced signal sequence is output from the circuit increases.

11. An information recording/reproducing encoding circuit according to Claim 5, wherein:

when the error code detection and correction by the first error-correction coding do not function and signal amplitude loss (dropout) with a predetermined code length is added to a reproduced signal sequence supplied from the recording medium, a burst length of code errors caused in a decoding result of an information code sequence is limited so that it is longer than the length of the added signal amplitude loss and is equal to or shorter than code sequence block length in case the predetermined code length exceeds a certain length equal to or shorter than code sequence block length.

12. An information recording/reproducing encoding circuit according to Claim 5, wherein:

in the error code detection and correction by the first error-correction coding, when a flag showing that error correction by the first error correction coding is impossible is sent out , time interval since a reproduced signal sequence is input to the circuit until the decoding result of an information code sequence for the reproduced signal sequence is output from the circuit increases.

13. An information recording/reproducing encoding circuit according to Claim 12, wherein:

the increase of time interval until the decoding result of the information code sequence for the reproduced signal sequence is output to the circuit is equal to or shorter than the time interval in which the

whole contents of a code sequence in the corresponding information data sector are output to the circuit.

14. An integrated circuit, wherein:

the information recording/reproducing encoding circuit according to Claim 3 is mounted.

15. A magnetic hard disk drive apparatus, wherein:

the information recording/reproducing encoding circuit according to Claim 3 or the integrated circuit according to Claim 14 is mounted.